REMARKS

Status of Claims:

Claims 1, 9, 11, 17 have been rejected.

Claims 1, 9, 11, 17 have been **amended** by this response.

The Examiner rejected claims 1, 11 under 35USC102 as being anticipated by Gallagher et al. (US Patent No. 5,640,343).

The Examiner stated "Gallagher et al disclose, in Fig. 2, a data storage device comprising an array of resistive memory cells having rows and columns; a set of diodes electrically connected in series to a plurality of memory cells in the array; a plurality of word lines (1-3) extending along the rows of the array; a plurality of bit lines (4-6) extending along the columns of the array; a first selected memory cell in the array (70); wherein the first selected memory cell is positioned between a first word line (1) in the plurality of word lines and a first bit line (4) in the plurality of bit lines; and a circuit (51 and 53) electrically connected to the array and capable of monitoring a signal current flowing through the first selected memory cell and comparing the signal current to an average reference current in order to determine which of a first resistance state and a second resistance state the first selected memory cell is in (see column 8, lines 38-51).

Applicants respectfully disagree with the Examiner for several reasons.

Amended claim 1 includes the following features:

an array of resistive memory cells having rows and columns;

a set of diodes electrically connected in series to a plurality of memory cells in the array;

a plurality of word lines extending along the rows of the array;

a plurality of bit lines extending along the columns of the array;

a first selected memory cell in the array, wherein the first selected memory cell is positioned between a first word line in the plurality of word lines and a first bit line in the plurality of bit lines; and

a circuit electrically connected to the array and capable of monitoring a signal current flowing through the first selected memory cell and comparing the signal current to an average reference current in order to determine which of a first resistance state and a second resistance state the first selected memory cell is in[.];

wherein the circuit is capable of obtaining the average reference current by placing an unselected memory cell in a first resistance state, sensing a first reference current while the unselected memory cell is in the first resistance state, placing the unselected memory cell in a second resistance state, sensing a second reference current while the unselected memory cell is in the second resistance state, and averaging the first reference current and the second reference current to obtain the average reference current.

The amendments to claim 1 are supported in the specification. More specifically, as stated on page 7, lines 3-9, "the circuit can obtain the average reference current value by monitoring resistive memory cells 170 other than the selected resistive memory cell 175. More specifically, the circuit can sometimes determine the average reference current value by performing portions of the triple sample sensing method on one or more other resistive memory cells 170 in the array 165 illustrated in FIG. 3 and can obtain an average reference current value to which the value of the current flowing through the selected resistive memory cell 175 may be compared."

Additionally, the specification describes the triple sense method on page 6, lines 3-10, "According to the triple sample sensing method, after obtaining the signal current value, the circuit obtains the average reference current value by placing the selected resistive memory cell 175 in a known first resistance state, such as the least resistive state or the state of greatest possible resistance. This may be done by altering the direction of

magnetization of the soft ferromagnetic layer 150 to be substantially either parallel or anti-parallel to the direction of magnetization of the fixed ferromagnetic layer 130. The circuit then records the value of a first reference current that flows through the selected restrictive memory cell 175 while it is in the known first resistance state.

The description of the triple sense method on page 6 is directed toward sensing a selected memory cell. However, the description on page 7 clearly states that the circuit can sometimes determine the average reference current value by performing portions of the triple sample sensing method on one or more other resistive memory cells 170 in the array 165.

Gallagher does not teach determination of an average current through the use of an unselected memory cell. None of the references suggest a triple sense method as described by the applicant.

The courts have ruled that "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. "Verdegall Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Also, "The identical invention must be shown in as complete detail as is contained in the ... claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

> None of the cited references teach "the circuit is capable of obtaining the average reference current by placing an unselected memory cell in a first resistance state, sensing a first reference current while the unselected memory cell is in the first resistance state, placing the unselected memory cell in a second resistance state, sensing a second reference current while the unselected memory cell is in the second resistance state, and averaging the first reference current and the second reference current to obtain the average reference current."

None of the references sense a resistance of an unselected memory cell using a triple-sense method as claimed.

The Examiner rejected claims 9, 17 under 35USC103(a) as being unpatentable over Gallagher et al. in view of Tran et al. (US Patent No. 6,385,111). The Examiner stated "Regarding claim 9, Gallagher et al. disclose, as applied in prior art rejection of claim 1, all claimed subject matter except the average reference current being obtained by monitoring memory cells other than the first selected memory cell.

Tran et al disclose, in FIG. 3, a memory cell being read by comparing its signal current (Is) to an average reference current (Ir) wherein the average reference current being obtained by monitoring memory cells (251-254) other than the first selected memory cell."

Tran (col. 4, lines 25-47) teaches the generation of reference currents Ira and Irb which are supplied to the reference input of a half-gain amplifier 126. As shown in Figure 1, the reference currents a generated by two separate bit lines 128, 130, and correspondingly, two separate reference cells.

To establish a prima facie case of obviousness, three basic criteria must be met.

First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the references or to combine reference teachings.

Second, there must be a reasonable expectation of success.

Finally, the prior art reference (or references when combined) must teach or suggest all claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. MPEP Sec. 2143, *In re vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Paralleling the MPEP references cited above, the Federal Circuit has enunciated several guidelines in making a 35USC103 obviousness determination.

A prima facie case of obviousness is established when and only **when the teachings from the prior art itself** would appear to have **suggested** the claimed subject matter to a person of ordinary skill in the art. *In re Bell,* 991 F.2d 783, 26 U.S.P.Q.2d 1529, 1531 (Fed Cir. 1993) (quoting *In re Rinehart*, 531 F.2d 1048, 1051 (C.C.P.A. 1976)). (Emphasis added). "The mere fact that the prior art **may** be modified in the manner suggested by the Examiner does **not** make the modification obvious unless the prior art suggested the desirability of the modification." (Emphasis added) In re Fritch, 23 USPQ 2d 1780, 1783-84 (Fed. Cir. 1992).

Here, the prior art references (or references when combined) do not teach or suggest all claim limitations. Additionally, there are no suggestions to modify the prior art to include the claim limitations.

More specifically, none of the references suggest "the circuit is capable of obtaining the average reference current by placing an unselected memory cell in a first resistance state, sensing a first reference current while the unselected memory cell is in the first resistance state, placing the unselected memory cell in a second resistance state, sensing a second reference current while the unselected memory cell is in the second resistance state, and averaging the first reference current and the second reference current to obtain the average reference current."

Claims 9 and 17 have been amended to further include the circuit being capable of obtaining the average reference current using a triple sample counter for determining the first reference current and the second reference current.

Support for amended claims 9, 17 can be found within the specification on page 6, lines 22-26 where the specification states "The sensing of the various currents discussed above may be performed through the sense amplifier 230, recorded through the triple sample counter 240, and emitted as an output signal 250. In some cases, higher-order data bits, such as "2" or "3" data bits, may also be stored in the data storage device, so long as the circuit is able to distinguish between the characteristic resistances of the higher-order data bits."

None of the cited references describe a triple sense method. Correspondingly, none of the references teach the use of a triple sample counter for determining the first reference current and the second reference current.

No new matter has been added by these amendments.

CONCLUSION

For the reasons given above, and after careful review of all the cited references, Applicant respectfully submits that none of the cited references, nor any combination of the cited references, will result in, teach or suggest Applicant's Claimed invention. But even if any such combination might arguably result in such Claimed invention, it is submitted that such combination would be non-obvious and patentable.

In view of the above Amendments and Remarks, Applicant has addressed all issues raised in the Office Action dated September 03, 2004, and respectfully solicits a Notice of Allowance for Claims 1, 9, 11, 17. Should any issues remain, the Examiner is encouraged to telephone the undersigned attorney.

It is believed that all of the pending Claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending Claims (or other Claims) that have not been expressed. Finally nothing in this paper should be construed as an intent to concede any issue with regard to any Claim, except as specifically stated in this paper, and the amendment of any Claim does not necessarily signify concession of unpatentability of the Claim prior to its amendment.

Applicant believes that no fees are currently due; however, should any fee be deemed necessary in connection with this Amendment and Response, the Commissioner is authorized to charge deposit account 08-2025, referencing the Attorney docket number 100111472-7.

Respectfully submitted,
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